Dr. M. Madhu Babu
Door No.11/945-2
2nd Cross Aravinda Nagar,
Ananthapuramu,
India, PIN – 515001.

Ph : +91 7036063777

Email :madhu07vlsi@gmail.com
madhubabu07.ece@jntua.ac.in

Professional Summary:

- **12.1 years** Working as Assistant Professor (Ad-hoc) in JNTUA College of Engineering (Autonomous)Ananthapuramu.
- **3.9 years** Worked as Assistant Professor in G. Pullareddy Engineering College (Autonomous), Kurnool.

Skills:

- Good knowledge on RTL coding (Verilog/ VHDL) and verification for FPGA / CPLD.
- Worked on different CAD tools like Synopsys, Cadence, Mentor Graphics, and Xilinx XST.
- Gate level, Transistor level design and implementation of digital integrated Circuits.
- Formal Verification and Static Timing Analysis.
- Excellent Team player.
- Involved in teams of small size and more responsibility.

Educational Qualification:

- Ph.D. Degree in the faculty of E.C.E for the thesis entitled, "Area and Power Efficient Variable Length Pipelined FFT / IFFT Architectures Using Fused Floating-point Operations" at JNTUA in March 2023.
- Master's Degree in VLSI System Design from VNR VJIET, JNTU Hyderabad in 2008.

Additional Qualifications:

- **UGC NET for Lectureship in Electronic Science** (UGC Ref. No 38684/NET-DEC, 2012), Lifelong Validity.
- **Peer Reviewer** for "**Wireless Personal Communications**", Springer Nature (New York, US), ISSN: 0929-6212.
- Received Certification of Appreciation "**NPTEL Discipline Star**" form Chairman & NPTEL Coordinator IIT Madras.

Experience Profile:

JNTUA CEA	Ananthapuramu	Sept. 2016–Till date	Assistant Prof. (Ad-hoc)
G.P.R.E.C	Kurnool	June'12–March'16	Assistant Prof.
JNTUA CEA	Ananthapuramu	June'09– May'12	Ad-hoc Lecturer
Sandeepani *(School of VLSI)*	Bangalore	Nov'08 – June'09	Project Trainee

Academic Profile:

Qualification	Institution	Year of Completion	Aggregate
Ph.D. (ECE, VLSI)	JNTUA, Ananthapuramu	2023	-
PG Diploma	Sandeepani (School Of VLSI), Bengaluru	2009	*71*
M. Tech.(VLSISD)	VNR VJIET, JNTU Hyderabad	2008	*70.34*
B. Tech. (E.C.E)	AITS, Rajampet, JNTU Hyderabad	2005	*66.44*
Intermediate	Crescent junior college, Anantapur	2001	*68.60*
SSC	L R G High School, Anantapur	1999	75.33

Technical Skills:

Synopsys Tools	Synopsys Verilog Compiler Simulator(VCS) Synopsys Design Compiler (DC Shell/SDC) Synopsys IC Compiler(ICC Shell) Synopsys Static Timing Analysis (Prime Time)
Cadence Tools	Spectre Circuit Simulator(Functional) Encounter(Place & Route), Virtuoso(Layout Suite), RTL to GDSII Implementation(IC), OrCAD/PSpice(Spice Programming).
Siemens EDA (Mentor Graphic) Tools	Modelsim 10.4 SE(Functional Verification), FPGA Advantage 6.3.(FPGA & ASIC Prototype) Design Architect IC Bundle(Design Complier), IC Station SDL Bundle(Place & Route), IC Trace Caliber XRC(Power), Layout Vs Schematic(LVS), ELDO Simulator(W Editor).

Xilinx Tools	Vivado 2012.2, Xilinx ISE 14.2, Xilinx ISE 10.1.03 Synthesis, Xilinx ISE 10.1.03 Implementation, Xilinx System Generator 10.1.03, Chip Scope Pro 10.1.03, Xilinx Plan Ahead 10.1.03, Xilinx Platform Studio SDK.
Software Language	C
HDL Languages	Verilog 1995-2001, VHDL-2008, System C
Scripting Language	TCL (Tool Command Language), Perl

Subjects Thought:

Undergraduate Courses	Postgraduate Courses
Electronic Devices and Circuits	CMOS Analog IC Design
Analog Electronics / Analog Circuits	CMOS Digital IC Design
Digital Electronics	Physical Design Automation
VLSI Technology	ASIC Design
Digital Design Through Verilog HDL	Low Power VLSI Design
Computer Architectures and Organization	FPGA Architecture and Applications
Electronic Devices and Circuits Lab.	Digital System Design Lab.
Analog Circuits Lab.	CMOS Digital IC Design Lab.
VLSI Design Lab.	CMOS Analog IC Design Lab.
Digital Design Through Verilog Lab.	Physical Design Automation Lab.

Publications: 30

International Journals: 15

1. **M. Madhu Babu** and K. Rama Naidu, "Area Efficient and Low Power Floating-Point FFT Processor for Next Generation Wireless Communication systems," Design Engineering (Toronto), Vol. 2021, Issue 06, Pp. 4825-4840, 2021.
2. **M. Madhu Babu** and K. Rama Naidu, "Area and power efficient fused floating-point dot product unit based on radix-2r multiplier & pipeline feedforward-cutset-free carry-lookahead adder," Information Technology in Industry, Vol. 09, Issue 02, Pp.782-788, April 2021.
3. **M. Madhu Babu** and G. Manjusha "Implementation of Efficient CORDIC Architecture using Binary Signed Digit Representation," GIS Science Journal, Vol. 09, Issue 07, ISSN:1869-9391, Pp:593-601, 2022.
4. N. Harinath Reddy and **M. Madhu Babu** "FGPA IMPLEMENTATION OF 4K POINT RADIX-4 MEMORY BASED FFT USING DSP SLICES," GIS Science Journal, Vol 09, Issue 05, ISSN: 1869-9391, Pp: 1091-1097, 2022.
5. K. Lokesh Babu and **M. Madhu Babu** "IP Verification of Inter Integrated Circuit(I2C) for Open Power Processor Based Fabless SoC" Mukt Shabd Journal, Vol. 11, Issue 12, ISSN: 2347-3150, Pp:219-223, 2022.
6. B. Sree Mangamma and **M.Madhu Babu** "Design an Approximate Multiplier Using 5:2 Compressor," INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN TECHNOLOGY, Vol 08, Issue 11, ISSN: , Pp: 447-453, 2022.
7. V.Ramakanth Reddy and **M.Madhu Babu** "Appurtenant Hardware Utilization of FFT for Real Input Samples," The International journal of analytical and experimental modal analysis, Vol. 11, Issue 08, Pp. 271-274, 2019.
8. G.Mounica, **M.Madhu Babu**, "On-Chip High Precision RC and LC Oscillators with Digital Compensation Technique In 45nm," International Journal of Advanced Computer Research (IJSAR), ISSN: 2349-7130,
9. P. Harshitha, **M. Madhu Babu**, "Implementation of Cordic Fixed Angle Rotation with Efficient Delay," International journal of Scientific Engineering and Technology Research (IJSETR), Vol.04, Issue 28, ISSN: 2319-8885, July 2015.
10. K.Kiran Kumar, **M.Madhu Babu**, "Radix-2^K Feed Forward FFT Architectures," International Journal of VLSI System Design and Communication Systems, Vol.02, Issue. 05, ISSN: 2322-0929, Pp. 0294-0298, August-2014.
11. K.Venkata Nagarjuna, **M.Madhu Babu**,"Low-Power Hybrid Flip-Flops and Implementation of Johnson Counter using Hybrid Flip-Flop," International Journal of VLSI System Design and Communication Systems, Vol.02, Issue. 05,ISSN: 2322-0929, , Pp. 0339-0345, August-2014.
12. G.Hari Kumar, **M.Madhu Babu**,"FPGA implementation of universal modulator using CORDIC algorithm for communication application," International Journal of Engineering Research and Development, e-ISSN: 2278-067X, p-ISSN: 2278-800X,Vol 6, Issue 11, PP. 08-14, April 2013.

13. N.Kavita, **M.Madhu Babu**, "Implementation of OFDM transmitter and receiver for FPGA based applications," Methods Enriching Power & Energy Developments,ISSN: 2230-7850, April 2013.
14. C.Sudhakar, **M.MadhuBabu**, "Design of E2 Framer and Deframer," International Journal of Science and Research (IJSR), Vol.04, Issue. 08, ISSN: 2319-7064, Pp.1846-49August 2015.
15. K.Sivanna, **M.Madhu Babu**, "Digital Down Converter (DDC) With CIC Filters For SDR Applications," International Journal of Advances in Engineering Research (IJAER), Vol. No. 2, Issue No. II, Ref.No.IJAER/9818, ISSN: 2231-5152, August 2011.

International Conferences: 14

1. V.Ramakanth Reddy, **M.Madhu Babu**, "Reliable Utilization of Hardware for the Real Valued FFT Architectures," IEEE International Conference on Intelligent Computing and Sustainable System, ICICSS-2019, August 20-22, 2019.
2. **M.Madhu Babu, K.Rama Naidu**, "Implementation of Multiplexers based Pipelined CORDIC for OFDM systems", IEEE International Conference On Recent Trends In Electronics Information Communication Technology, May 20-21, 2016, India
3. K.V.Hemanth Babu, **M.Madhu Babu**, "Design of Weighted Modulo 2n+ adder With Optimized area and Delay Using Simple Correction Schemes", International Conference on Computer Science and Information Technology, CSIT-2011.
4. Marchandeya Gupta, **M.Madhu Babu**, "Low Power Coding Approach for Error Free Coding Technique in VLSI Design", International Conference on Electronics and Communication Engineering, ICECE-2011.
5. D.Vijay Dinesh Babu, **M.Madhu Babu**, "FPGA Hardware Architecture of the Steganographic ConText Technique", International Conference on Nanosciences, Engineering & Advanced Computing, ICNEAC-2011.
6. C.Naresh, **M.Madhu Babu**, "Enhancing Spectrum Efficiency of Cognitive Radio waveforms Using SD-SNSE Frame work",*2nd International Conference on Control, Communication & Computer Technology,CCCT-2011.*
7. Mounika Reddy Bojja, **M.Madhu Babu**, "Demand Response Thermostat", *International Conference on Technology and Managament, ICTM-2011.*
8. Suresh Babu, **M.Madhu Babu**, "Implementation of Median filter Using FPGA", *2nd International Conference on Signals, Systems & Automation ICSSA-2011.*
9. S.B.Rukahna Sultana, **M.Madhu Babu**, "A Lifting Based Parallel VLSI Architecture For Image Compression Using 2D Discrete Wavelet Transform", *Guru Nanak Engineering College, Emerging trends in Signal Processing and VLSI Design-2010.*
10. **M.Madhu Babu**, Bollam Abhinay, "Evaluation Of Sensor Networks Using Economical Pipelined MIPS," *OXFORD College Of Engineering*, ICODC- 2010.
11. M.V.Sruthi, **M.Madhu Babu**, "High Speed Encryption and Decryption Of Blowfish", ARUNAI Engineering Collage, *NOVEL Applications of Nano Technology, NANO-T10.*

12. B,Swathi, **M.Madhu Babu**, "Implementation Of Low Power Audio Subword Sorter Unit For Audio Streaming Applications."
13. B.Naga Rajesh, **M.Madhu Babu**, "Demising OF CFA Images For Single Sensor Digital color Cameras Using PCA", ARUNAI Engineering Collage, *NOVEL Applications Of Nano Technology, NANO-T10.*
14. **M.Madhu Babu**, "Improving Error Tolerance And Access Efficiency Based on Memory Soft Redundancy", International Conference of Reliability, Infocom Technology and Optimization, ICRITO-2010.

National Conferences: 01

1. M.V.Sruthi, **M.Madhu Babu** "High Speed Encryption and Decryption Of Blowfish." NOVA College Of Engineering & Technology, NET-2K10.

Workshops/FDPS: 28

1. "**Telco to Techno: Building Sustainable, Autonomous Networks with Open Source & AI**" by Atul Deshpande organized by IEEE-IISc VLSI Chapter and ComSoc Chapter on January 24, 2025.
2. "**No Risk RISC-V: Perspective of a Microarchitecture Researcher in RISC-V Era**" by Dr. Debjyoti Bhattacharjee organized by IEEE-IISc VLSI Chapter on January 10, 2025.
3. "**The Evolution of Power Management ICs in Semiconductor Industry**" by Prof. Qadeer Khan organized by IEEE-IISc VLSI Chapter on January 5, 2025.
4. "**Opto-Electronic Transceiver Array for Low-power and High Bandwidth Density Wireline Links**" by Devesh Khilwani organized by IEEE-IISc VLSI Chapter on January 3, 2025.
5. "**Design Innovation for Silicon-based D-band Phased Arrays**" by Dr. Wooram Lee organized by IEEE-IISc VLSI Chapter on July 26, 2024.
6. "**Recent Advances on Low Phase Noise mm Wave Oscillators**" by Dr. Prof. Andrea Bevilacqua organized by IEEE-IISc VLSI Chapter on July 11, 2024.
7. "**Electronic Systems Design: Hands-On Circuits and PCB Design with CAD Software**" by NPTEL-AICTE Faculty development Programme (Funded by the MoE, Govt. of India) July-Oct. 2024 (12 Weeks).
8. "**Design Innovation for Silicon-based D-band Phased Arrays**" by Dr. Wooram Lee organized by IEEE-IISC VLSI Chapter on July 26, 2024.
9. "**Recent Advances on Low Phase Noise mmWave Oscillators**" by Dr. Prof.Andrea Bevilacqua organized by IEEE-IISC VLSI Chapter on July 11, 2024.
10. "**System Design Through Verilog**" by NPTEL-AICTE Faculty development Programme (Funded by the MoE, Govt. of India) July-Sept. 2023 (8 Weeks).
11. "**VLSI to System Design: Silicon to End Application Approach**" organized by All India Council for Council for Technical Education (AICTE), Arm Education and STMicroelectronics from July 31st to 4th August 2023.
12. "**Drone Technology**," Five-day FDP jointly organized by IIITDM Kurnool & JNTUA Ananthapuramu under the project Capacity Building for Human Resources Development in Unmanned Aircraft System (Drone and related Technology), MeitY, Govt. of India in association with AP Higher Education Planning Board (Anantapur Region Cluster), Conducted at JNTUA College of

Engineering (Autonomous), Ananthapuramu, Andhra Pradesh during the period: 17th – 21st July 2023.

13. "**Microsoft Azure Fundamentals**", Organized by JNTUA Ananthapuramu and Microsoft Corporation India in association with Andhra Pradesh State Council of Higher Education under the Faculty Empowerment program on New Technologies on 20th June 2022.
14. "**Microsoft Azure AI Fundamentals**", Organized by JNTUA Ananthapuramu and Microsoft Corporation India in association with Andhra Pradesh State Council of Higher Education under the Faculty Empowerment program on New Technologies on 21st June 2022.
15. "**Digital VLSI Design and Verification**", Five day workshop organized by department of ECE, Bangalore Institute of Technology in association with Entuple Technologies and IEEE-BIT CAS from 23rd – 27th August 2021.
16. "**Development of MOOCs and Production Techniques**", Two day workshop organized under TEQIP-III conducted by JNTUA College of Engineering (Autonomous), Ananthapuramu during 17th – 18th January 2020.
17. "**Recent Advancements in XILINX and ASIC Designs**", MeitY, Govt. of India, Sponsored One Week Faculty Development Programme (FDP), Organized by the E & ICT Academy, National Institute of Technology, Warangal Conducted at JNTUA College of Engineering (Autonomous), Ananthapuramu, Andhra Pradesh during 16th - 21st December 2017.
18. *"**SOC-based Physical design using CADENCE tools**"*, two-day workshop conducted by GPREC, Kurnool, 4th – 5th March 2016.
19. "**Present Education System**"**,** One-day workshop Faculty Development Program, conducted by NPTEL Madras at GPREC, Kurnool, Dec 2015.
20. "***Hands-on experience on Intel Atom Processor***", a two-day workshop conducted by GPREC, Kurnool in collaboration with INTEL Corporation Ltd. Hyderabad, Nov.2015.
21. "***PSOC using Cadence Tools***", two days workshop conducted by GPREC Kurnool in collaboration with CADENCE Corporation Ltd. Nov 2014.
22. "**Instructional Excellence in Intelligent Systems**", three day courseware, practical training and evaluations under the Intel College Excellence Program conducted in G. Pulla Reddy Engineering College, Kurnool From 17th – 19th April 2014.
23. "**Analog and Digital CMOS Design Flow using Mentor Graphics EDA Tools Training Programme**", two day National Level Workshop Organized by Development of Electronics and Communication Engineering, G. Pulla Reddy Engineering College (Autonomous), Kurnool on 28th - 29th November 2012.
24. Participated in the National Seminar on "**Wireless Networking and Communications, WN&C'12**" Sponsored by APSCHE & UGC held during 27th – 28th January 2012.
25. "***Low-Power Design and Test***", two days course conducted by VLSI Society of India, Hyderabad 30th – 31st July 2007.
26. *"**Design of Embedded System Applications-DES 2007***" Short Term Intensive Course organized by VNE VJIET Hyderabad on 26th – 28th Feb. 2007.
27. *"**Nano Electronics**"*, conducted by Industry Institute Partnership Cell(IIPC) 2006, CBIT Hyderabad.

28. *"**Main Member of the Organizing committee of ELEFIESTA-2004**", conducted by Annamacharya Institute of Technology and Sciences. National Level Students paper Conference, 2004, Kadapa.*

Patents Published/Granted:

S.No.	Application Number	Title of the Patent	Date published
1.	202421080062A	Automated Solar Charging Station for Electric Vehicles	22/11/2024

Books/Book Chapters: 01

1. A Research Book on "**FFT/IFFT Architectures Using Fused Floating-point Operations – Area and Power Efficiency Variable Length Pipelined FFT/IFFT architectures**", Mallepalli Madhu Babu, Kurukundu Rama Naidu, LAP LAMBERT Academic Publishing, April 2023.

Projects Guided:

1. M.Tech. Projects – 32
2. B.Tech. Projects – 19

Certification Courses: 18

NPTEL Online Certifications (9)	1. **Electronic Systems Design: Hands-On Circuits and PCB Design with CAD Software** (IITM) Jul-Oct. 2024 (12-week course) 2. **Basic Electrical Circuits** (IITH) Jul-Oct. 2024 (12-week course) 3. **BFLI-002: FRENCH Exchanger / Interactions (French)** (IGNOU Delhi) July-Oct. 2024 (4-weeks course) 4. **Analog Circuits** (IITD) Jan-March 2024 (8-week course) 5. **Microprocessor and Microcontrollers** (IIT Khar) Jan-April 2024 (12-week course) 6. **Digital Circuits** (IIT Khar) Jul-Oct 2023 (12-weeks course) 7. **System Design Through Verilog** (IITG) Jan-April 2023 (8-week course) 8. **Digital System Design** (IITM) Jan-April 2023 (12- week course) 9. **BFLI 001: PARLER DE SOI /Talking About Oneself (French)** (IGNOU Delhi) Jan-April 2023 (4-weeks course)
edX Verified Certificates (8)	1. **Introduction to Microprocessors** by Arm Education 2. **Computer Architecture Essentials on Arm** by Arm Education 3. **Introduction to ChatGPT, Boost your productivity to the maximum using artificial intelligence** by Universitat Politecnica de Valencia 4. **HTML5 and CSS Fundamentals** by World Web Consortium 5. **AI Applications and Prompt Engineering** by by The Linux Foundation 6. **Business Considerations for 5G with Edge, IoT and AI** by The Linux Foundation 7. **Open Source and the 5G Transition** by The Linux Foundation 8. **Frances Introductorio** by Universidades Anahuac
edX Professional Certificates (1)	1. **5G Strategy for Business Leaders** by Linux Foundation

Membership of Scientific / Engineering Bodies:

1. Member IETE (F-504017)
2. Member IEI(I) (M-161025-7)
3. Member ISTE (LM108629)
4. Member IEEE (93196788)
5. Member of VLSI Society of India (M No. P23#TD0108#MER1028593)

Academic Identities:

1. ORCID: https://orcid.org/0000-0003-0713-8814
2. Scopus ID: 57193571481
3. Web of Science Researcher ID: AAK-8067-2021
4. Google Scholar ID: 5wwMJDwAAAAJ
5. Vidwan ID: https://vidwan.inflibnet.ac.in/profile/320099

I hereby declare that all the details furnished above are appropriate and liable up to the best of my knowledge.

(Dr. M. Madhu Babu)